Prolonged 500 °C Operation of 6H-SiC JFET Integrated Circuitry

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Abstract: This paper updates the long-term 500 °C electrical testing results from 6H-SiC junction field effect transistors (JFETs) and small integrated circuits that were introduced at ICSCRM-2007. Two packaged JFETs have now been operated in excess of 7000 hours at 500 °C with less than 10% degradation in linear I-V characteristics. Several simple digital and analog demonstration integrated circuits successfully operated for 2000-6500 hours at 500 °C before failure.

Introduction

NASA is developing very high temperature semiconductor integrated circuits (ICs) for beneficial use in the hot sections of aircraft engines and for Venus exploration. Additional applications for electronics that can operate at temperatures greater than 300 °C include automotive engines and deep-well drilling [1]. In order for beneficial technology insertion to occur, such transistor ICs must be capable of prolonged operation in such harsh environments. This paper reports on the long-term 500 °C electrical characterization of 6H-SiC integrated circuits based on epitaxial n-channel 6H-SiC junction field effect transistors (JFETs) with 10 µm gate lengths. The fabrication of these devices (including IC formation using single-level metal interconnect) and the first 2000 hours of 500 °C transistor and amplifier IC operation was introduced at ICSCRM-2007 [2]. This paper presents additional results obtained as testing has progressed to longer operating times and expanded to additional demonstration circuits, including digital logic gates.

Experimental Results

Experimental procedures including JFET cross-section, fabrication and packaging processing, and measurement setups have been previously described elsewhere [2-8].

Discrete JFETs. Fig. 1 compares drain current I_D versus drain voltage V_D characteristics of a packaged 200µm/10µm JFET measured by source-measure units (SMUs) during the 1st and 7014th hours of 500 °C operation under V_D = 50 V and gate bias V_G = -6 V. Similar results were obtained for the 100µm/10µm JFET measured by a digitizing 60 Hz curve-tracer continuously operated with 50 V drain bias sweeps and -2V gate steps from V_G = 0 V to V_G = -16 V. Fig. 2 illustrates the measured variation of DC on-state current I_{DSS}, transconductance g_m, drain-to-source resistance R_{DS}, and V_T for both packaged JFETs as a function of 500 °C

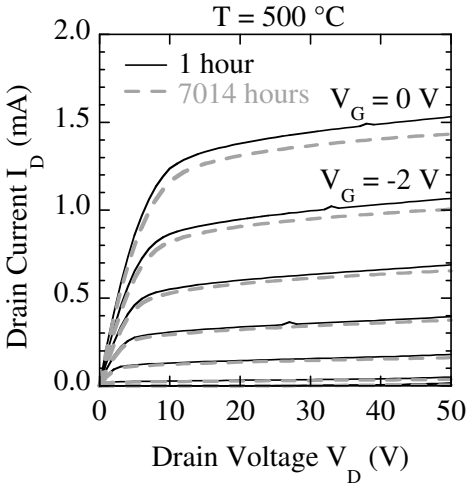

Fig. 1. I_D vs. V_D characteristics of packaged 200µm/10µm 6H-SiC JFET measured during the 1st and 7014th hour of 500 °C testing.

operating time up to 7000 hours. The Fig. 2 plots are normalized to each transistor's measured value of I_{DSS0}, g_{m0}, R_{DS0}, and V_{T0} recorded at the 100 hour mark of 500 °C testing (i.e., after "burn-in" [3]). Fig. 2a shows I_{DSS} recorded at V_D = 20V, V_G = 0V. Fig. 2b shows the g_m benchmarked at V_D = 20 V from V_G = 0V and -2V steps, and Fig. 2c shows the time evolution of R_{DS} for V_G = 0V. (In Refs. [4,5] R_{DS} for V_G = -2V was mistakenly shown for 100µm/10µm device.) It is important to note that the y-axis scale limits for Fig. 2a-c plots are set to ±10% of each parameter's measured 100-hour value. With the exception of a few data points from the curve-tracer-measured 100µm/10µm JFET, the Fig. 2 data falls within this 10% parameter variation window. Fig. 2d shows the precise time variation of V_T extracted from the computer-fit x-intercept of the SMU-measured $\sqrt{I_D}$ vs. V_G of the 200µm/10µm JFET. The measured V_T changes by less than 1%. This excellent stability reflects the fact that JFET V_T is determined by the as-grown 6H-SiC epilayer structure. These two devices are still demonstrating good functionality as on-going 500 °C testing continues. Similar testing of three more discrete JFET's has been initiated with similar initial results for the first 1000 hours of 500 °C operation.

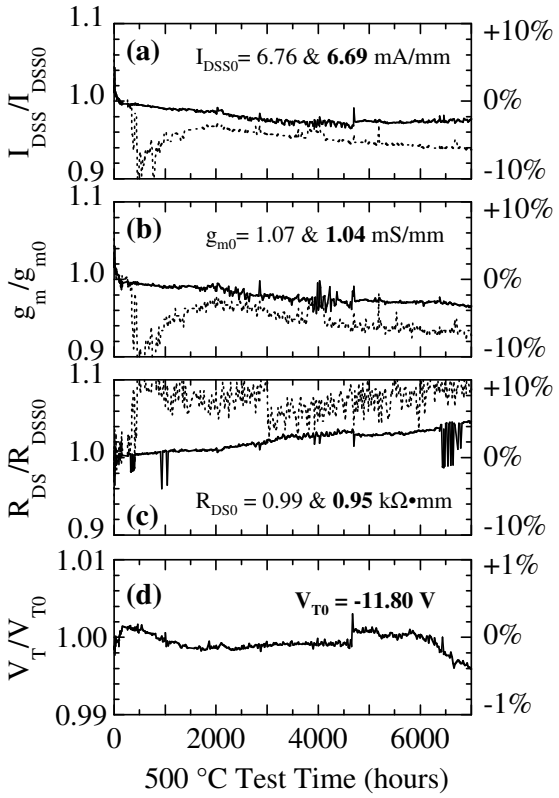

Fig. 2. Normalized (see text) JFET parameters vs. 500 °C test time for packaged devices with 100µm/10µm gate (dashed, plain text, measured by curve-tracer) and 200µm/10µm gate (solid, **bold text**, SMU-measured).

Integrated Circuits. A 6H-JFET differential amplifier (diff-amp) IC with two JFETs and three epitaxial resistors [2] was successfully operated at 500 °C for over 6500 hours before failing. Fig. 3 shows nearly identical raw waveforms recorded by a digitizing oscilloscope during the first and 6519th hour of 500 °C testing. Fig. 4 plots the measured 1 kHz voltage gain vs. 500 °C operating time. For unknown reasons the diff-amp gain spiked some (~ 20%) between 1050 and 1600 hours, but afterwards, the amplifier gain stabilized with negligible apparent drift until an initial failure occurred at 6519 hours. A few days after initial failure, the diff-amp resumed operation, albeit at slightly higher gain until total circuit failure was registered at 7337 hours. Failure analysis of this circuit has not yet been

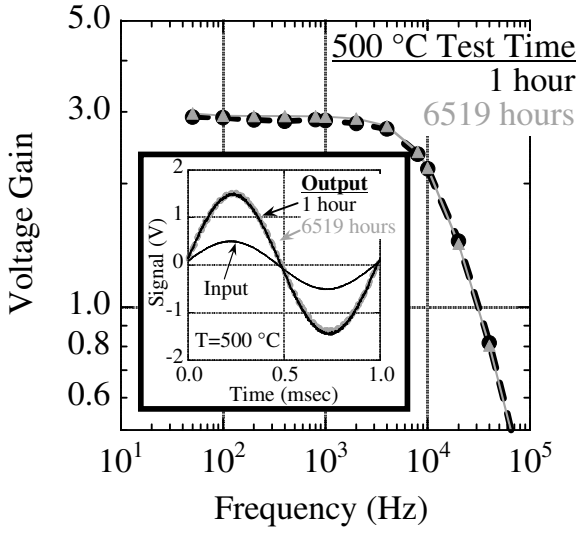

Fig. 3. Diff-amp IC voltage gain vs. frequency (and 1 kHz waveforms, inset) measured during 1st and 6519th hours of 500 °C testing.

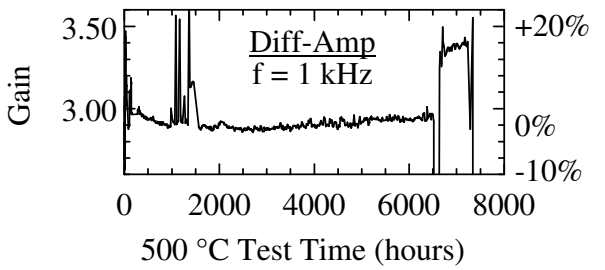

Fig. 4. Diff-amp IC low-frequency (1 kHz) voltage gain vs. 500 °C operating time.

initiated due to the fact that other devices (JFETs) on the same circuit board remain under test at 500 °C.

Fig. 5 summarizes the measured and SPICE-modeled gain vs. frequency characteristics of a simple inverting amplifier stage circuit at 24 °C and 500 °C. The nearly temperature-independent low-frequency gain arises from the fact that resistance R_{DD} and transistor g_m are oppositely linked to the conductivity of the 6H-SiC n-channel layer, which for these devices exhibits ~ $T^{-1.3}$ (in degrees Kelvin) behavior [5,6]. The observed decline in the operating frequency with increasing temperature is primarily due to the decreasing conductivity of the 6H-SiC n-channel layer. These results indicate that relatively straightforward future device and circuit optimizations (such as scaling transistors to smaller dimensions) will yield improved circuit capability and frequency performance. This inverting amplifier stage operated for over 3900 hours before sudden failure.

Digital logic gate integrated circuits fabricated on this wafer have also demonstrated unprecedented 500 °C durability. A digital NOR gate demonstrated over 2400 hours of operation at 500 °C [3,4] while a digital NOT gate (Fig. 6) functioned over 3600 hours at 500 °C [4,5]. These logic circuits use negative logic voltages, but work over the entire 25 °C to 500 °C temperature range without changes to power supply voltages. More demanding long-term tests (such as repeated thermal cycling) are being initiated as additional chips are custom-packaged for 500 °C operation.

The fact that no discrete JFETs failed while all integrated circuits failed over the same 500 °C testing duration suggests that the observed circuit failures are due to degradation of the metal/dielectric interconnect stack. Fig. 7 compares the optical appearance of (a) an as-fabricated chip, and (b) a packaged chip that was exposed to thousands of hours of 500 °C operation. Significant physical changes occurred to the air-exposed interconnect metallization during the 500 °C test, especially in the vicinity of the gold wire bonds. Initial probe testing of metal traces across two failed chips has documented a few examples of separate interconnect traces demonstrating poor electrical isolation from each other. These near-short circuits indicate that loss of dielectric layer insulating property occurred in at least some localized regions. This probe testing has also revealed a few examples of near-open (poor conductance) interconnect traces. To date there has been no observed failure of packaging or gold wire bonds, and only one failure of an ohmic contact to an n-type SiC epitaxial resistor. Recently initiated materials analysis of failed chips should enable important insights into root chemical and physical mechanisms causing chip failures so that they may be reported and mitigated in future work.

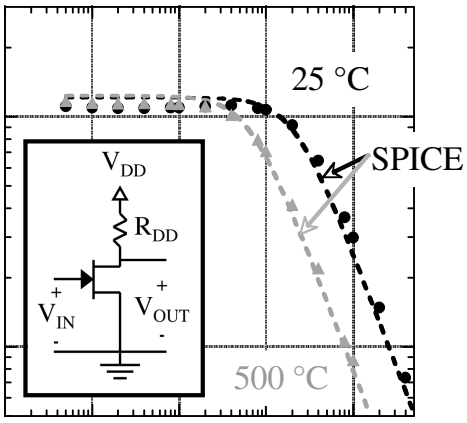

Fig. 5. Inverting amplifier gain vs. frequency at 25 °C and 500 °C [5].

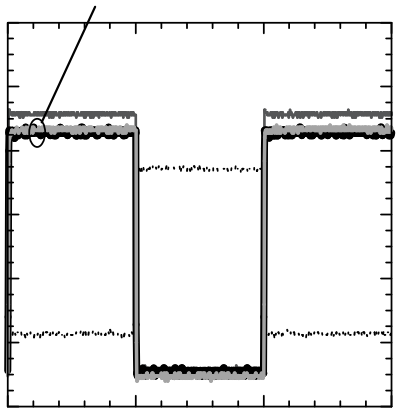

Fig. 6. Waveforms demonstrating operation of digital NOT gate IC at 25 °C and at the beginning and end of prolonged 500 °C test [5].

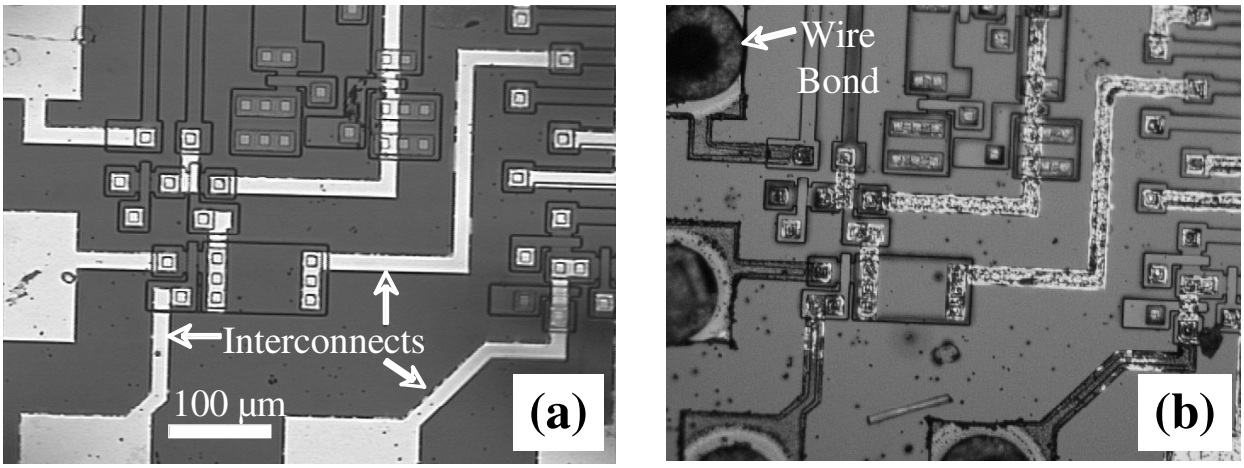

Fig. 7. Optical micrographs of portions of NOT gate IC chips. (a) An as-fabricated chip prior to packaging. (b) A packaged chip following failure after thousands of hours operating at 500 °C.

Summary

The increased 500 °C transistor and IC durability and stability demonstrated in this work is now sufficient for sensor signal conditioning circuits in jet-engine test programs. Although only a small number of devices have been packaged and tested for thousands of hours at high temperature, this demonstration establishes the feasibility of producing SiC integrated circuits that are capable of prolonged 500 °C operation. This result was achieved through the integration of fundamental materials and/or processing advancements, including the development of high temperature n-type ohmic contacts [7] and high temperature packaging technology [8]. Shrinkage of device dimensions and implementation of multilayer interconnects are obvious important further steps towards realizing durable 500 °C SiC integrated circuitry with increased functionality.

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